Homework 1

(Due date: January 21st @ 11:59 pm)

Presentation and clarity are very important!

PROBLEM 1 (25 PTS)

a) Simplify the following functions using ONLY Boolean Algebra Theorems. For each resulting simplified function, sketch the logic circuit using AND, OR, XOR, and NOT gates. (15 pts).

- ✓ $F(x,y,z) = \prod(M_1, M_2, M_4, M_6)$
- ✓ $F = \overline{B(\bar{C} + \bar{A}) + \overline{AB}}$
- ✓ $F = \overline{(x \oplus \bar{y})z + xy\bar{z}}$

b) For the following Truth table with two outputs: (10 pts)

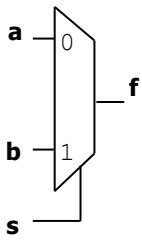
- Provide the Boolean functions using the Canonical Sum of Products (SOP), and Product of Sums (POS). (4 pts)
- Express the Boolean functions using the minterms and maxterms representations.
- Sketch the logic circuits as Canonical Sum of Products and Product of Sums. (4 pts)

x	y	z	f_1	f_2
0	0	0	0	1
0	0	1	0	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	1	1
1	1	1	1	0

PROBLEM 2 (13 PTS)

a) The following circuit (trapezoid) has the following logic function: $f = \bar{s}a + sb$.

- Complete the truth table of the circuit and sketch the logic circuit. (3 pts)



s	a	b	f
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

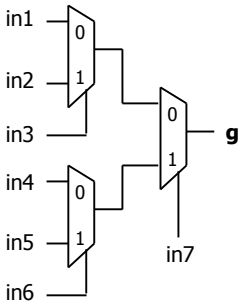
b) We can use several instances of the previous circuit (trapezoid) to implement different functions. (10 pts)

- For the given inputs, provide the resulting function g (minimize the function).

in1	in2	in3	in4	in5	in6	in7
x_1	0	x_3	1	0	x_1	x_2

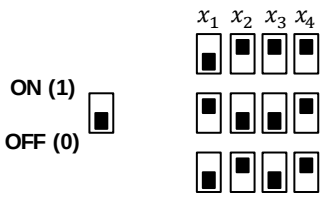
- The following selection of inputs generate the function: $g = x_1x_2 + x_2x_3$. Demonstrate that this is the case.

in1	in2	in3	in4	in5	in6	in7
0	x_3	x_2	0	1	x_2	x_1



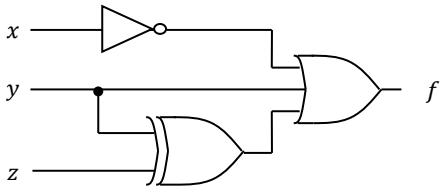
PROBLEM 3 (11 PTS)

- Security combinations: A lock opens ($z = 0$) when the 4 switches (x_1, x_2, x_3, x_4) are set in any of the 3 configurations shown in the figure, otherwise the lock is closed ($z = 1$). A switch generates a '1' in the ON position, and a '0' in the OFF position.
  - ✓ Provide the simplified Boolean equation for the output z and sketch the logic circuit.



PROBLEM 4 (26 PTS)

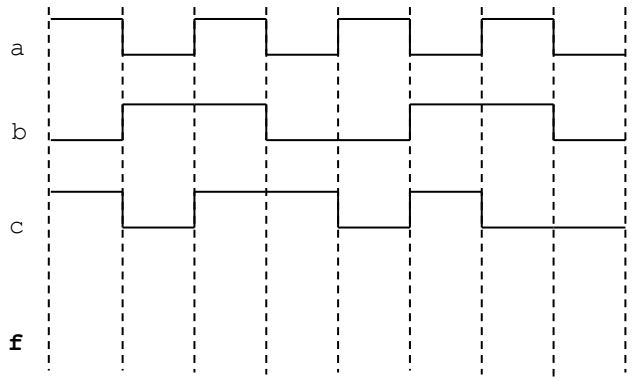
a) Complete the truth table describing the output of the following circuit and write the simplified Boolean equation (6 pts).



x	y	z	f
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

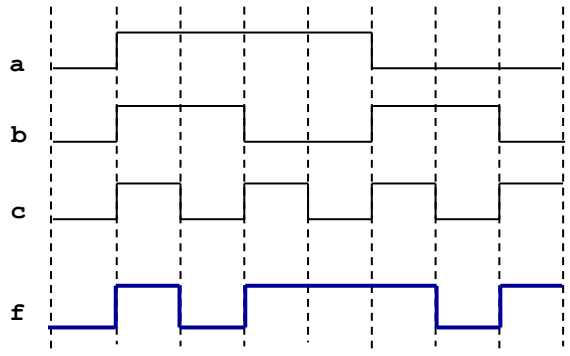
b) Complete the timing diagram of the logic circuit whose VHDL description is shown below: (6 pts)

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port ( a, b, c: in std_logic;
         f: out std_logic);
end circ;

architecture st of circ is
  signal x, y: std_logic;

begin
  x <= b xor (not a);
  f <= y nand (not b);
  y <= x nor c;
end st;
```

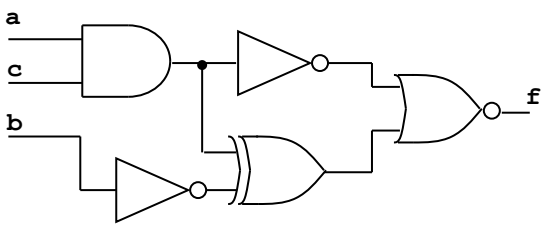


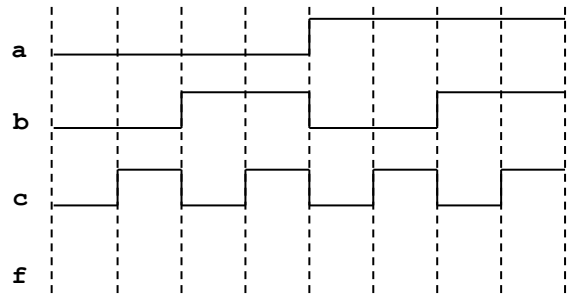
c) The following is the timing diagram of a logic circuit with 3 inputs. Sketch the logic circuit that generates this waveform. Then, complete the VHDL code. (8 pts)

```
library ieee;
use ieee.std_logic_1164.all;

entity wav is
  port ( a, b, c: in std_logic;
         f: out std_logic);
end wav;

architecture st of wav is
-- ???
begin
   -- ???
end st;
```



d) Complete the timing diagram of the following circuit: (6 pts)

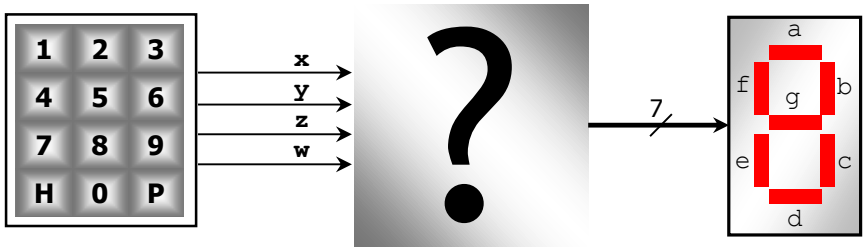




PROBLEM 5 (25 PTS)

- A numeric keypad produces a 4-bit code as shown below. We want to design a logic circuit that converts each 4-bit code to a 7-segment code, where each segment is an LED: A LED is ON if it is given a logic '1'. A LED is OFF if it is given a logic '0'.

✓ Complete the truth table for each output (a, b, c, d, e, f, g). (4 pts)
✓ Provide the simplified expression for each output (a, b, c, d, e, f, g). Use Karnaugh maps for c, d, e, f, g and the Quine-McCluskey algorithm for a, b. Note that it is safe to assume that the codes `1100` to `1111` will not be produced by the keypad.



Value	X	Y	Z	W	a	b	c	d	e	f	g
0	0	0	0	0							
1	0	0	0	1							
2	0	0	1	0							
3	0	0	1	1							
4	0	1	0	0							
5	0	1	0	1							
6	0	1	1	0							
7	0	1	1	1							
8	1	0	0	0							
9	1	0	0	1	1	1	1	1	0	1	1
P	1	0	1	0							
H	1	0	1	1							
	1	1	0	0							
	1	1	0	1							
	1	1	1	0							
	1	1	1	1